The isolated SPI module is designed for applications, where SPI signals need to be transferred over longer distances than usually. It is based on Linear’s LTC6820. The board is designed as two layer stack-up, with GND plane on the bottom layer and signal traces and components at the top layer. Signals and power are supplied over standard 100mil (2.54mm) pitch IDC header.

Figure 1: photo of the board
License

This board is licensed under the open hardware license CERN OHL v1.2. All documentation are available at www.maleetronic.com for download.

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Please feel free to give your highly appreciated feedback, comments and suggestions. Or ask any questions about the product. We’ll be glad to answer or help you.
Specification

- Dimension: 40.005 mm x 30.099 mm (1.575” x 1.185”)
- 1 Mbps Isolated SPI Data Communication at 10m
- 500 kbps Isolated SPI Data Communication at 100m
- Galvanic Isolation Barrier using standard transformer (1500V)
- Requires no software changes in most SPI systems
- 3.5V to 15V power supply
- SPI mode can be adjust via on-board jumpers
- can act as Master or Slave (adjustable via jumper)
- screw terminal for twisted pair cable (i.e. as in CAT5 Ethernet cable)

For more details and description, please read the data sheet of the LTC 6820. Below is an possible application scenario of the module.

Figure 2: Application

http://www.maleetronic.com
Jumper Settings & Pin header

Pin Header P1

P1 is the pin header for the SPI signals and power supply. It has a standard pitch of 100 mils (2.45 mm).

<table>
<thead>
<tr>
<th>PIN</th>
<th>SIGNAL</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MOSI</td>
<td>SPI Signals</td>
</tr>
<tr>
<td>1</td>
<td>MISO</td>
<td>SPI Signals</td>
</tr>
<tr>
<td>1</td>
<td>SCK</td>
<td>SPI Signals</td>
</tr>
<tr>
<td>1</td>
<td>CS</td>
<td>SPI Signals</td>
</tr>
<tr>
<td>1</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>VDD</td>
<td>Digital Supply Voltage (Output U3)</td>
</tr>
<tr>
<td>1</td>
<td>VS</td>
<td>Supply Voltage (Input U3)</td>
</tr>
</tbody>
</table>

You can supply about 3.5V to 15V to the board. The on-board LDO LTC1763 will generate 3.3V for supply the LTC 6820. For more details, see the specification for the LTC 1763.

In case you need different voltage levels for the SPI signals, you can supply 2.7V to 5.5V to the board via VDD pin(P1[6]). In this case you should remove U3 (LTC1763). It is also possible to use any other pin compatible power supply with 8-SOIC footprint or ones from the same family. See the data sheet for the LTC1763 for more details.

It is also possible to use the board with two different SPI signal levels(level shifting).
Jumper P2, Master & clock speed

With P2 you adjust the clock frequency and the Master/Slave mode.

![Jumper Settings Master, Slow]

Figure 3: Jumper Settings Master, Slow

SLOW pin

For clock speeds below 200 kHz, the jumper must be in position 1-3(VDD). For clock frequencies 200-1000 kHz, the jumper must be in position 3-5(GND).

<table>
<thead>
<tr>
<th>POSITION</th>
<th>VOLTAGE LEVEL</th>
<th>CLOCK FREQUENCY</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-3</td>
<td>VDD</td>
<td>&lt;200 kHz</td>
</tr>
<tr>
<td>3-5</td>
<td>GND</td>
<td>200-1000 kHz</td>
</tr>
</tbody>
</table>

MSTR pin

For using this board as SPI Master, the jumper must be in position 2-4 (VDD). For using this board as SPI Slave, the jumper must be in position 4-6 (GND). The default position is 4-6 (Slave).

<table>
<thead>
<tr>
<th>POSITION</th>
<th>VOLTAGE LEVEL</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-4</td>
<td>VDD</td>
<td>Master</td>
</tr>
<tr>
<td>4-6</td>
<td>GND</td>
<td>Slave</td>
</tr>
</tbody>
</table>
**Jumper P3, SPI MODE**

With P3 you adjust the SPI mode. Phase and Polarity.

![Jumper Settings SPI Mode](image)

**Figure 4: Jumper Settings SPI Mode**

<table>
<thead>
<tr>
<th>MODE</th>
<th>POL</th>
<th>PHA</th>
<th>POSITION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>5-3, 6-4</td>
<td>SCK Idles Low, Latches on Rising Edge</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>5-3, 4-2</td>
<td>SCK Idles Low, Latches on Falling Edge</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>3-1, 6-4</td>
<td>SCK Idles High, Latches on Rising Edge</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>3-1, 4-2</td>
<td>SCK Idles High, Latches on Falling Edge</td>
</tr>
</tbody>
</table>

Table 4: Jumper P3, SPI mode
Screw Terminal P4

The screw terminal P4 is the connector for the twisted pair cable. The differential signal pulses are transferred or received over this connector on IP and IM. Connect IP with IP and IM with IM respectively.

Bias Resistors R1, R2

The bias resistors are selected for a good compromise between power consumption and noise immunity. Ib is set to 0.5mA, which is good for most application and allow for 50m cable length with a normal CAT5 twisted pair. If you need/want to change these resistors, read the data sheet the section ”Application Information” for more details how to calculate these resistors.
Attachments

1. Board Schematics
2. CERN OHL v1.2
3. CERN OHL v1.2 How-to-Guide
CERN Open Hardware Licence v1.2

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